Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.040”**

**.040”**

**Top Material: Al**

**Backside Material: Au**

**B = .007” X .008”**

**E = .009 X .014”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP325V**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 8/3/18**

**MFG: CENTRAL SEMI THICKNESS .007” P/N: 2N5320**

**DG 10.1.2**

#### Rev B, 7/1